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Bidirectional voltage level translators NVT2001/02/03/04/06/08/10, PCA9306, GTL2000/02/03/10

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Document information

Info	Content
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Abstract	NXP Voltage Translators are used in bidirectional signaling voltage level translation applications for I/O buses with incompatible logic levels. The NVT20001, NVT2002, NVT2003, NvT2004, NVT2006, NVT2008, NVT2010, GTL2000, GTL2002, GTL2003, GTL2010 and PCA9306 voltage translation devices can be operational from 1.0 V to 3.6 V at $V_{CC(A)}$ (low voltage side) and 1.8 V to 5.5 V at $V_{CC(B)}$ (high voltage side) without direction control for open-drain or push-pull I/O devices. Device operation, resistor sizing and typical applications are discussed in this application note.

Revision history

Rev	Date	Description
v.1	20120404	application note; initial version

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1. Introduction

There are many I/O standards that have different voltage level requirements for the input voltage (V_{IH} or V_{IL}) and output voltage (V_{OH} or V_{OL}) typically based on the device operating voltage. The different technologies available in circuit design determine the input voltage threshold and output voltage level achievable in different devices. In order to interface two devices of differing technologies successfully, voltage level translation is needed and certain requirements must be met:

1. The V_{OH} of the driving device must be greater than the V_{IH} of the receiving device.
2. The V_{OL} of the driving device must be less than the V_{IL} of the receiving device.
3. The output voltage from the driving device must not exceed the I/O voltage tolerance of the receiving device.

Providing a migration path is important in all industry segments because system components used in new low-power designs must communicate with components using the existing bus infrastructure even if they are operating at higher voltage levels. Since new low-power devices are designed and produced with advanced sub-micron semiconductor process technologies, there has to be an easy way to prevent damage to the new low-power device and translate voltage switching levels of the higher voltage legacy device as shown in Figure 1.

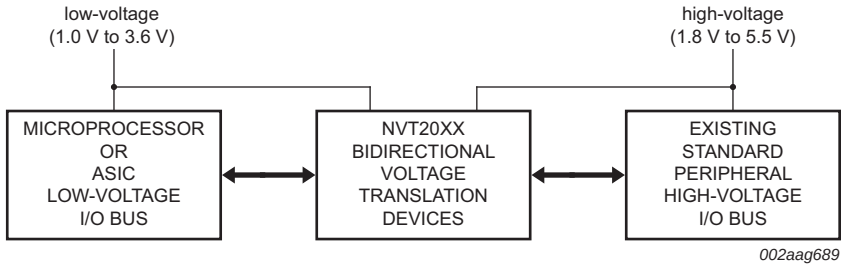


Fig 1. Typical bidirectional voltage-translation application

2. Product offering

The NVT2001, NVT2002, NVT2003, NVT2004, NVT2006, NVT2008, NVT2010, GTL2000, GTL2002, GTL2003, GTL2010 and PCA9306 devices are offered in a wide range of bit widths and packages as shown in Table 1. They are available in 1-, 2-, 3-, 4-, 6-, 8-, 10-, or 22-bit widths and package sizes ranging from the TSSOP, HVQFN and DHVQFN packages to the extremely thin small XSON, XQFN and HXSON packages. This allows the designer maximum flexibility in picking the bit width and package that is best suited for them.

Table 1. Bidirectional voltage level translator product summary

Device name	Number of I/O pairs	Pin count	Packages							
			SO	VSSOP	XSON	TSSOP	XQFN	HXSON	HVQFN	DHVQFN
NVT2001	1	6	-	-	NVT2001GM (XSON6)	-	-	-	-	-
NVT2002	2	8	-	-	NVT2002GD (XSON8U)	NVT2002DP (TSSOP8)	-	-	-	-
PCA9306[1]	2	8	PCA9306D (SO8)	PCA9306DC PCA9306DC1 (VSSOP8)	PCA9306GD1 (XSON8U) PCA9306GF (XSON8)	PCA9306DP PCA9306DP1 (TSSOP8)	PCA9306GM (XQFN8)	-	-	-
GTL2002	2	8	GTL2002D (SO8)	GTL2002DC (VSSOP8)	-	GTL2002DP GTL2002DP/Q900 (TSSOP8)	GTL2002GM (XQFN8U)	-	-	-
NVT2003	3	10	-	-	-	NVT2003DP (TSSOP10)	-	-	-	-
NVT2004	4	12	-	-	-	-	-	NVT2004TL (HXSON12U)	-	-
NVT2006	6	16	-	-	-	NVT2006PW (TSSOP16)	-		NVT2006BS (HVQFN16)	NVT2006BQ (DHVQFN16)
NVT2008	8	20	-	-	-	NVT2008PW (TSSOP20)	-	-	-	NVT2008BQ (DHVQFN20)
GTL2003	8	20	-	-	-	GTL2003PW (TSSOP20)	-	-	-	GTL2003BQ (DHVQFN20)
NVT2010	10	24	-	-	-	NVT2010PW (TSSOP24)	-	-	NVT2010BS (HVQFN24)	NVT2010BQ (DHVQFN24)
GTL2010	10	24	-	-	-	GTL2010PW (TSSOP24)	-	-	GTL2010BS (HVQFN24)	-
GTL2000	22	48	-	-	-	GTL2000DGG (TSSOP48) GTL2000DL (SSOP48)				

[1] PCA9306 is the same design and function as NVT2002 for SMBus voltage level translator with more packages available.

3. Key features and benefits

The NXP family of voltage level translators has several key features that benefit a system designer when designing an interface between devices with different I/O voltage levels. the NVT20xx family of devices has a lower R_{on}, C_{io}, and higher ESD rating than the GTL2000/2002/2003/2010 and PCA9306. The GTL2000/2002/2003/2010 also have a higher $V_{CC(B)}$ to $V_{CC(A)}$ (SREF) voltage difference rating for operation without a pull-up resistor on the A-side (S-side). For the GTL2000/2002/2003/2010, $V_{CC(B)} - V_{CC(A)} \geq 1.5$ V, where the PCA9306 and NVT20xx family $V_{CC(B)} - V_{CC(A)} \geq 1.0$ V is needed for operation without a pull-up resistor on the A-side. Table 2 provides a summary of the features and benefits of the NXP level translator family.

Table 2. NXP level translator family features and benefits

NXP level translator features and benefits	Description
Easy PCB trace routing	Bn and An I/O pairs are matched on either side of the devices (flow through pinout); this makes it easier to route signals to and from the device
Allow wide signal supply range between An and Bn ports	signal supply range between 1.0 V to 3.6 V (An) and 1.8 V to 5.5 V (Bn)
Minimal channel-to-channel deviation and skew	all the transistors are on one die with same electrical characteristics; this is a benefit over discrete transistor voltage translation solution
Easy migration to lower voltages (for example, 1.0 V or 1.2 V)	system designer just changes the $V_{CC(A)}$ voltage without modifying any circuit design
Lowest 5 μA standby current is perfect for mobile application	only required standby current for reference transistor with both $V_{CC(A)}$ and $V_{CC(B)}$ supply voltages
Less than 1.5 ns maximum propagation delay	accommodates Standard-mode and Fast-mode I^2C-bus devices and multiple masters
Low ON-state resistance	The NVT20xx and PCA9306 have the lowest ON-state resistance at 3.5 Ω, while the GTL2000/2002/2003/2010 have an ON-state resistance of 6.5 Ω.
Open-drain I/O ports	provides bidirectional voltage translation with no direction pin
High level of ESD protection	The NVT20xx provides 4 kV of ESD protection (HBM). The GTL2000/2002/2003/2010 and PCA9306 provide 2 kV.

4. What is a voltage translator and how it works

The NVT2001, NVT2002, NVT2003, NVT2004, NVT2006, NVT2008, NVT2010, GTL2000, GTL2002, GTL2003, GTL2010 and PCA9306 are functionally the same, however the electrical characteristics are slightly different, such as the R_{on}, C_{io}, and the ESD protection. A distinction of the GTL2000/2002/2003/2010 is that the $V_{CC(B)}$ to $V_{CC(A)}$ (SREF) voltage difference rating for operation without a pull-up resistor on the A-side (S-side) is $V_{CC(B)} - V_{CC(A)} \geq 1.5$ V, where the PCA9306 and NVT20xx $V_{CC(B)}$ to $V_{CC(A)}$ voltage difference rating for operation without a pull-up resistor on the A-side is only $V_{CC(B)} - V_{CC(A)} \geq 1$ V. The NXP voltage translator family can be used for bidirectional level translation, but do not provide capacitance isolation. These devices do not need a direction control signal if both sides of driving devices are open-drain outputs. Each device consists of an array of matching N-channel pass transistors with their gates tied together internally at the EN pin, as shown in Figure 2. All of the transistors are fabricated on one integrated die. This leads to a very small fabrication-process variation in the

electrical characteristics of the transistors. Therefore, there is minimal deviation from one output to another in voltage or propagation delay. Also, the NXP voltage translator family is designed such that the source and drain are interchangeable, where either side of the FET can be used as the low-voltage side. Because of these reasons, our solutions are preferred over discrete devices.

The NXP voltage level translators work by connecting one of the FETs (Field-Effect Transistors) as a reference transistor, and the remainder as pass transistors. The low-voltage side (A1 to An) is the source of the FET, while the high-voltage side (B1 to Bn) is the drain of the FET. The voltage of the reference device at the low-voltage side limits the remainder of the pass transistors to that voltage level.

Operating a voltage translator with the minimum number of external components requires that:

- For the PCA0306 and NVT200xx, the $V_{CC(A)}$ input must be less than or equal to $V_{CC(B)} - 1$ V to bias the reference transistor into conduction. For the GTL2000/2002/2003/2010 $V_{CC(A)}$ (SREF) input must be less than or equal to $V_{CC(B)} - 1.5$ V.
- The gate of the reference transistor is tied to its drain ensure that the FETs are operating in the saturation region.

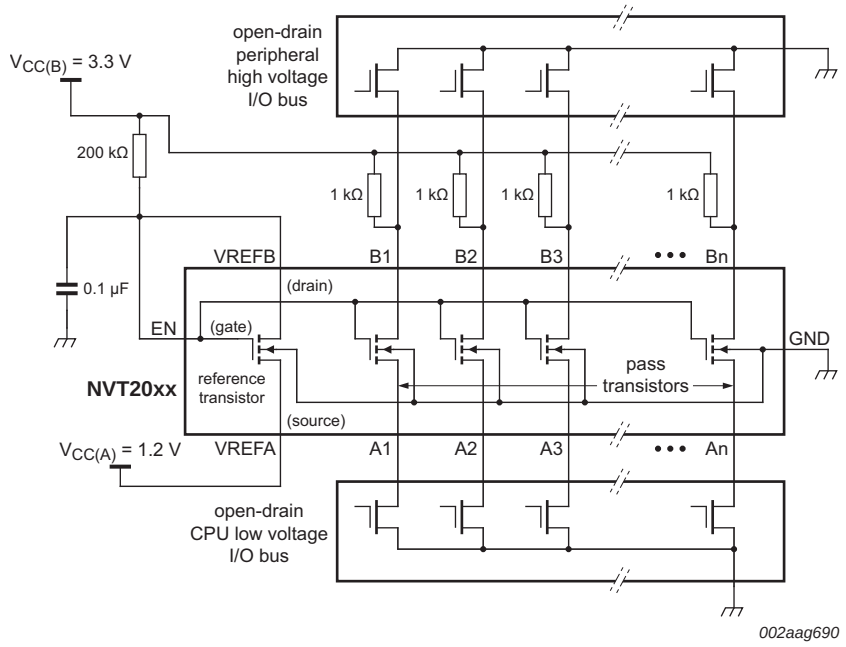


Fig 2. Simplified schematic of a typical NVT20xx device

The reference transistor along with a resistor sets V_{bias} and the gate voltage (V_G) of all the pass transistors. The gate voltage is determined by the characteristic gate-to-source voltage difference (V_{GS}) and it can vary between 0.6 V and 1 V, so $V_G = V_{CC(A)} + V_{GS}$. The low-voltage side of the pass transistors is limited to the $V_{CC(A)}$. If the $V_{CC(B)} - V_{CC(A)} \leq 1$ V, then a pull-up resistor is required on A-side to ensure the An outputs reach the $V_{CC(A)}$ voltage level.

When either An or Bn port is driven LOW, the FET is turned ON and a low resistance path exists between the An and Bn port. The low ON-state resistance (R_{on}) of the pass transistor allows connections to be made with minimal propagation delay.

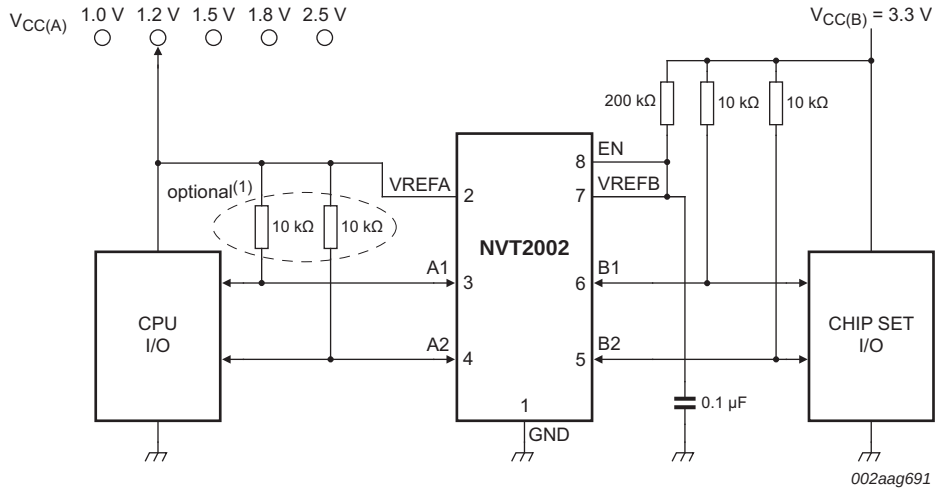
When the Bn port is driven or pulled HIGH, the voltage on the An port is limited to the $V_{CC(A)}$. When the An port is driven or pulled HIGH, the Bn port is pulled to supply voltage $V_{CC(B)}$ by the pull-up resistors. In the example shown in Figure 2, $V_{CC(A)}$ is set equal to the I/O voltage level of the CPU, whereas $V_{CC(B)}$ is set to the voltage level desired on the I/O voltage of the peripheral device.

This allows a seamless translation between higher and lower voltages selected by the user without the need for directional control.

When EN is connected through a 200 kΩ pull-up resistor to a $V_{CC(B)}$ high voltage supply, and the An and Bn I/Os are connected, the translator switch is ON, allowing bidirectional data flow between ports. When EN is pulled LOW, the transistor switch is OFF and a high-impedance or disconnect state exists between ports. The voltage level translators protect new lower voltage devices from the overvoltage and ESD conditions applied by the older, higher voltage legacy devices and translate the V_{IH} and V_{OH} switching levels easily.

5. Applications

Since bidirectional voltage level translators are passive devices, pull-up resistors may be needed depending on the external I/O interface type (totem pole, push-pull or open-drain) and the translation direction (HIGH-to-LOW direction, LOW-to-HIGH direction, or bidirectional). The NVT20xx devices allow translations between any voltages from 1.0 V to 5.5 V as long as the voltage difference between the $V_{CC(B)}$ and reference source ($V_{CC(A)}$) voltages is greater than 1 V. The gate (EN) and reference drain (VREFB) must connect together through a 200 kΩ resistor to a $V_{CC(B)}$ voltage, as shown in Figure 3. A filter capacitor (0.1 μF) on VREFB is recommended. This circuit biases the gate above the reference source voltage, $V_{CC(A)}$, and provides some filtering from any noise.



(1) 10 kΩ pull-up resistors are required if $V_{CC(B)} - V_{CC(A)} < 1$ V.

Fig 3. Typical 2-bit bidirectional application

5.1 Open-drain I/Os and bidirectional translation

For bidirectional translation, the drivers on both sides of any level translator must be open-drain outputs or they must be controlled so that contention between a HIGH level on an output driver on one side and a LOW level on the other side is prevented. When using open-drain devices, it is always required to use pull-up resistors at B-side, and they must be sized so as not to overload the output drivers. When using the PCA9306 or NVT20xx family, if $V_{CC(B)} - V_{CC(A)} < 1$ V, then pull-up resistors are required on A-side to pull up the An outputs to $V_{CC(A)}$. It is important to note that if pull-up resistors are required on both the A-side and B-side, the equivalent pull-up resistor value becomes the parallel combination of the two resistors when the pass transistor is ON. If $V_{CC(B)} - V_{CC(A)} \geq 1$ V, then pull-up resistors on the A-side are not required.

When using the GTL2000/2002/2003/2010 family, if $V_{CC(B)} - V_{CC(A)} < 1.5$ V, then pull-up resistors are required on A-side (S-side) to pull up the An (Sn) outputs to $V_{CC(A)}$. It is important to note that if pull-up resistors are required on both the A-side (S-side) and B-side (D-side), the equivalent pull-up resistor value becomes the parallel combination of the two resistors when the pass transistor is ON. If $V_{CC(B)} - V_{CC(A)} \geq 1$ V, then pull-up resistors on the A-side (S-side) are not required.

5.2 Multiple voltages bidirectional translation

The bidirectional voltage level translators allow the use of different bus voltages on each source to drain channel so that a low voltage device can communicate with multiple different high voltage devices without any additional protection. The example in Figure 4 shows how the NVT2006 can be used in a bidirectional I²C-bus and uni-directional SPI application where the microcontroller (left side) operating at 1.8 V can interface to higher voltage devices (right side) operating at 3.3 V for SPI slave device and 5.0 V for I²C-bus slave device. Since the voltage difference between the low voltage ($V_{CC(A)}$ = 1.8 V) and the high voltage (V_{CC2} = 5 V) on the 200 kΩ resistor for the EN (gate) is higher than 1.0 V, so pull-up resistors on the low voltage side (1.8 V) are not required.

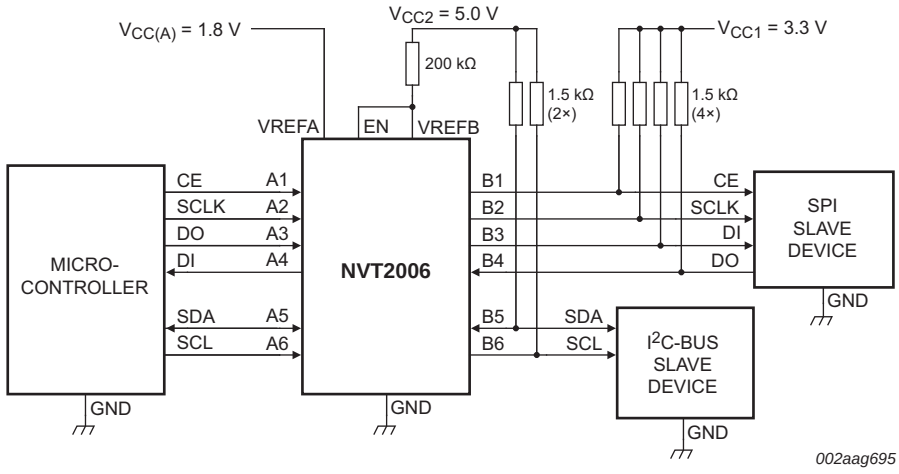


Fig 4. Bidirectional multiple voltage I²C-bus/SPI application

5.3 Push-pull I/Os and uni-directional translation

The NXP family of voltage translators can support push-pull or totem pole I/Os, however great care must be taken for them to work properly. They can operate in either down or up uni-directional translation, but the push-pull I/O must be the only driver on the bus. If they are used in push-pull bidirectional control, then there must be a direction control bit controlling which I/O is acting on the bus. If this is not the case, then a bus contention can arise and the operation of the level translator will be compromised.

5.3.1 Down translation (from Bn to An uni-direction)

When doing down translation, there is no driver on the lower voltage side, the higher voltage driver may be either totem pole (push-pull) without any pull-up resistor or open-drain with a pull-up resistor. If $V_{CC(B)} - V_{CC(A)} < 1$ V, a pull-up resistor is needed on the low voltage side. The value of the pull-up resistor can be calculated by equations in Section 6.

5.3.2 Up translation (from An to Bn uni-direction)

When a totem pole (push-pull) driver or open-drain driver with or without pull-up resistors on the low-voltage side may be used, a pull-up resistor is always required on the high voltage side to get the full HIGH level. The resistor values must be chosen so as not to overload the pull-down driver. The value of the pull-up resistor can be calculated by equations in Section 6.

6. How to size pull-up resistor value

Sizing the pull-up resistor on an open-drain bus is specific to the individual application and is dependent on the following driver characteristics:

- The driver sink current
- The V_{OL} of driver
- The V_{IL} of the driver
- Frequency of operation

The following sections detail calculations that can be made for different use cases so that the minimum resistance for the pull-up resistor can be found.

6.1 Driver sink current derating

In order for a solution to operate correctly, $V_{OL} \leq V_{IL}$, but if the rated V_{OL} of a driver is higher than the V_{IL} of the input that it is driving, the solution must be modified. Typically, the pull-up resistor value must be increased to ensure that the relationship of $V_{OL} \leq V_{IL}$ is satisfied. When V_{OL} is reduced below what is specified, then the rated current drive is lessened. Therefore, it is important to understand the relationship between the drive current and V_{OL}. It can be assumed that the drive strength is linearly derated as a function of voltage. Equation 1 represents the derating of the driver current strength if the V_{OL} must be lower than what is specified.

$$I_o = \left(\frac{I_{OL}}{V_{OL}}\right) V_{IL} \quad (1)$$

Where:

I_o is the estimated derated output current.

I_{OL} is the specified output drive strength.

V_{IL} is the input LOW threshold voltage that the driver must drive down to in order to operate correctly.

V_{OL} is the output LOW voltage that the driver is driven to as an output.

A normalized plot of I_o can be seen in Figure 5 for a 0.4 V rated V_{OL} device.

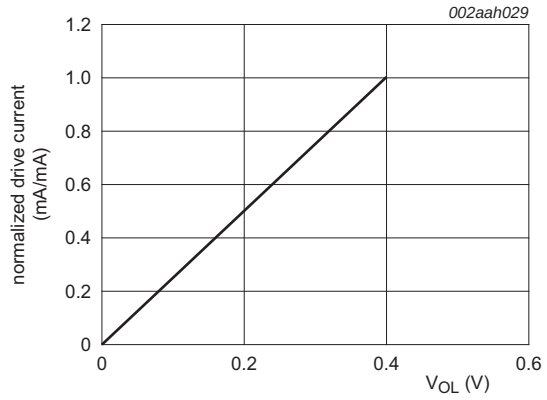


Fig 5. Derating curve for normalized drive current versus V_{OL}, when V_{OL} is specified at 0.4 V

If the specified V_{OL} is lower than the required V_{IL}, then it is safe to use the specified I_{OL} current without any modifications. When using the calculations found in this document, it is assumed that either V_{OL} is lower than V_{IL}, or that the drive current strength has been derated for a lower V_{OL}.

6.2 Pull-up resistor estimation when $V_{CC(B)}$ minus $V_{CC(A)}$ is greater than or equal to 1 V

When $V_{CC(B)} - V_{CC(A)} \geq 1$ V, the following calculation can be made to determine the lowest value of resistance needed to operate the bus correctly, based on the following operating conditions and a few assumptions:

- $V_{CC(A)} = 1.5$ V
- $V_{CC(B)} = 3.3$ V
- $V_{OL(A)} = V_{IL(A)} = V_{CC(A)} \times 10\ \% = 0.15$ V

  where $V_{OL(A)}$ is the output LOW of the A-side bus master and $V_{IL(A)}$ is the input LOW threshold of the A-side bus master
- $V_{OL(B)} = V_{IL(B)} = V_{CC(B)} \times 10\ \% = 0.33$ V

  where $V_{OL(B)}$ is the output LOW of the B-side bus device and $V_{IL(B)}$ is the input LOW threshold of the B-side bus device
- $I_{D(A)}$ = 10 mA drive strength is assumed to be already scaled for V_{OL} as detailed in Section 6.1

- $I_{D(B)}$ = 15 mA drive strength is assumed to be already scaled for V_{OL} as detailed in Section 6.1
- R_{sw} = 3 Ω
- Pull-up resistors are needed on the B-side only
- Device chosen is PCA9306 or NVT20xx family. When GTL2000/2002/2003/2010 is used, substitute 1 V with 1.5 V.

The minimum resistor value is determined from the higher of the two values from Equation 2 and Equation 3, derived from summing the currents at pins A1 and B1. When the A-side is pulled LOW, the condition will exist that the $V_{OL(A)}$ is lower than the $V_{IL(B)}$, so the solution will operate correctly. The voltage at B1 must be equal to $V_{OL(A)}$ plus the voltage drop across the switch. Equation 2 calculates $R_{pu(B)}$ when the A-side is asserted, the current path is shown in Figure 6. $I_{D(A)}$ is equal to the A-side driver sink current.

$$R_{pu(B)} = \frac{V_{CC(B)} - V_{OL(A)}}{I_{D(A)}} - R_{sw} = \frac{3.3\ V - 0.15\ V}{10\ mA} - 3\ \Omega = 312\ \Omega \quad (2)$$

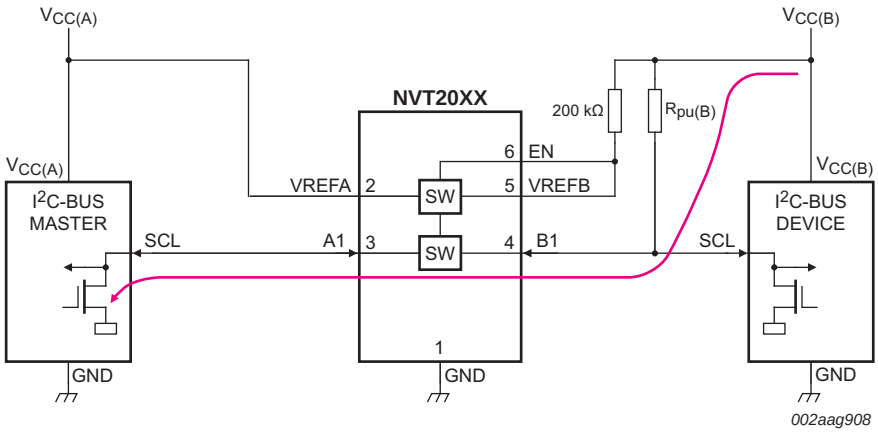


Fig 6. Current path through NVT20xx when A-side driver is turned on and $V_{CC(B)} - V_{CC(A)} \geq 1$ V

When the B-side is pulled LOW following the above assumptions, the condition will exist that the specified $V_{OL(B)}$ is higher than the $V_{IL(A)}$, so in order for the solution to operate, $V_{OL(B)}$ is lowered to be equal to $V_{IL(A)}$ in order for the I/O to register a LOW. Therefore, the voltage at B1 must be calculated to be $V_{IL(A)}$. Since no current flows through the switch, the voltage at B1 equals the voltage at A1, and the I/O is satisfied. The current path is shown in Figure 7. $I_{D(B)}$ is equal to the B-side driver sink current.

Equation 3 calculates $R_{pu(B)}$ when the B-side is asserted.

$$R_{pu(B)} = \frac{V_{CC(B)} - V_{IL(A)}}{I_{D(B)}} = \frac{3.3\ V - 0.15\ V}{15\ mA} = 210\ \Omega \quad (3)$$

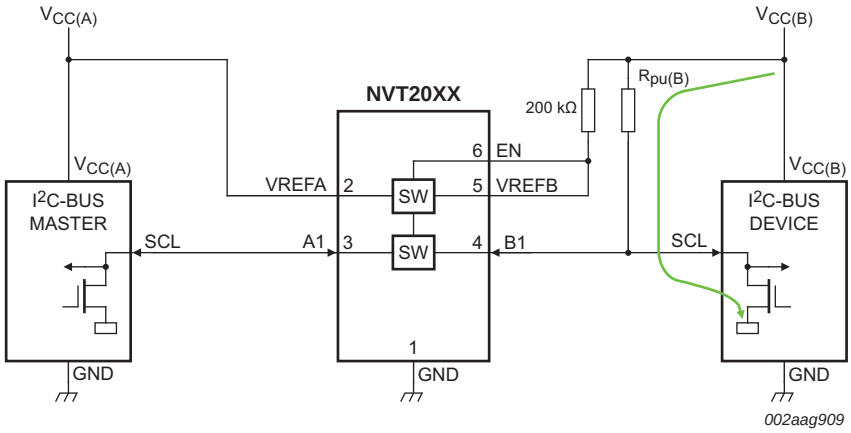


Fig 7. Current path through NVT20xx when B-side driver is turned on and $V_{CC(B)} - V_{CC(A)} \geq 1$ V

For this example the smallest resistance that can be used and still meet the V_{OL} and V_{IL} requirements is 312 Ω.

Table 3, Table 4 and Table 5 contain suggested minimum values of pull-up resistors for typical voltage translation levels and drive currents. The calculated values assume that both drive currents are the same. $V_{OL} = V_{IL} = 0.1 \times V_{CC}$ and accounts for a ±5 % V_{CC} tolerance of the supplies, ±1 % resistor values. It should be noted that the resistor chosen in the final application should be equal to or larger than the values shown in Table 3, Table 4 or Table 5 to ensure that the pass voltage is less than 10 % of the V_{CC} voltage and the external driver should be able to sink the total current from the pull-up resistor. When selecting the minimum resistor value from these tables, the lowest drive current strength seen in the application should be used.

6.3 Pull-up resistor estimation when $V_{CC(B)}$ minus $V_{CC(A)}$ is less than 1 V

When $V_{CC(B)} - V_{CC(A)} < 1$ V, the following calculation can be made to determine the lowest value of resistance needed to operate the bus correctly.

The following three equations (Equation 4, Equation 5 and Equation 6) are derived from summing the currents at pins A1 and B1. When the A-side is asserted, drive current must equal the sum of the currents through the pull-up resistors and voltage at A1 must be equal to $V_{OL(A)}$. It must also be true that $V_{OL(A)}$ must be lower than $V_{IL(B)}$, if not, then $V_{IL(B)}$ must be substituted for $V_{OL(A)}$. Equation 4 shows the sum of the current through $R_{pu(A)}$ and $R_{pu(B)}$ that equals the A-side driver sink current. The current paths are illustrated in Figure 8.

$$I_{D(A)} = \frac{V_{CC(A)} - V_{OL(A)}}{R_{pu(A)}} + \frac{V_{CC(B)} - V_{OL(A)}}{R_{pu(B)} + R_{sw}} \quad (4)$$

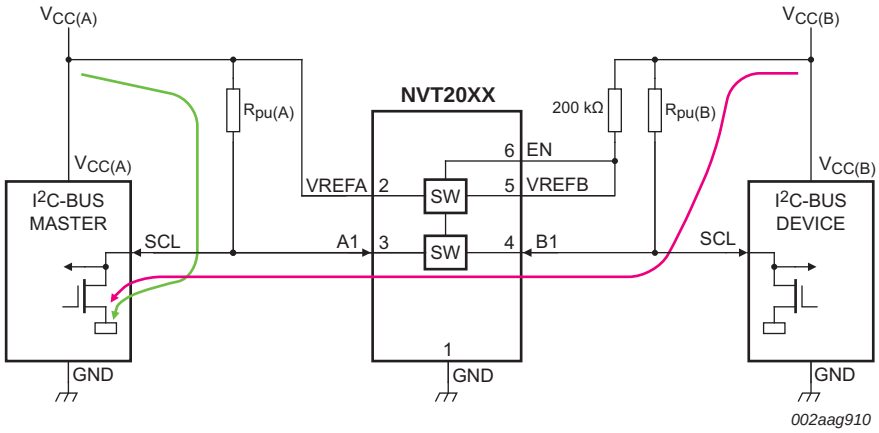


Fig 8. Current path through NVT20xx when A-side driver is driven LOW and $V_{CC(B)} - V_{CC(A)} < 1$ V

When the B-side is asserted, the condition may exist that the specified $V_{OL(B)}$ is higher than the $V_{IL(A)}$, so in order for the solution to operate, we must ensure that $V_{OL(B)}$ is lowered to be equal to $V_{IL(A)}$ in order for the I/O to register a LOW. Therefore, the voltage at B1 must be calculated to be $V_{IL(A)}$. So the voltage at B1 must be $V_{IL(A)}$ minus the voltage across the switch, since a current path exists through the transistor.

Equation 5 shows the sum of the current through $R_{pu(A)}$ and $R_{pu(B)}$ that equals the B-side driver sink current. The current paths are illustrated in Figure 9.

$$I_{D(B)} = \frac{V_{CC(A)} - V_{IL(A)}}{R_{pu(A)}} + \frac{V_{CC(B)} - V_{x(B)}}{R_{pu(B)}} \quad (5)$$

where

$$V_{x(B)} = V_{CC(A)} - \left(\frac{V_{CC(A)} - V_{IL(A)}}{R_{pu(A)}}\right) \times (R_{pu(A)} + R_{sw}) \quad (6)$$

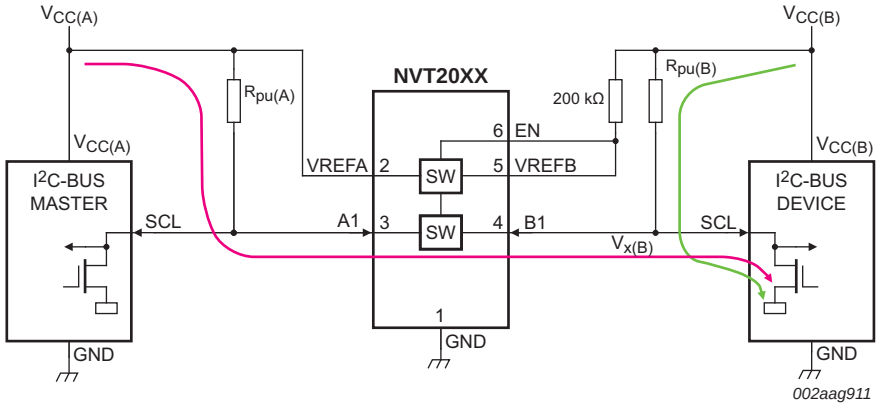


Fig 9. Current path through NVT20xx when B-side driver is driven LOW and $V_{CC(B)} - V_{CC(A)} < 1$ V

The pull-up resistor value can be solved for when Equation 4, Equation 5 and Equation 6 are simplified by making the following assumptions:

- $V_{CC(A)}$ = 2.5 V
- $V_{CC(B)}$ = 3.3 V
- $V_{OL(A)} = V_{IL(A)} = V_{CC(A)} \times 10\ \% = 0.25$ V

  where $V_{OL(A)}$ is the output LOW of the A-side bus master and $V_{IL(A)}$ is the input LOW threshold of the A-side bus master
- $V_{OL(B)} = V_{IL(B)} = V_{CC(B)} \times 10\ \% = 0.33$ V

  where $V_{OL(B)}$ is the output LOW of the B-side bus device and $V_{IL(B)}$ is the input LOW threshold of the B-side bus device
- $I_{D(A)}$ = 10 mA drive strength is assumed to be already scaled with V_{OL} as detailed in Section 6.1
- $I_{D(B)}$ = 15 mA drive strength is assumed to be already scaled with V_{OL} as detailed in Section 6.1
- R_{sw} = 0 Ω[1]
- Pull-up resistors are needed on both the A-side and B-side
- $R_{pu(A)} = R_{pu(B)} = R_{pu}$
- Device chosen is a PCA9306 or NVT20xx family. When GTL2000/2002/2003/2010 is used, substitute 1 V with 1.5 V.

The minimum resistance value is then determined from the higher of the two values from the following equations (Equation 7 and Equation 8), where $I_{D(A)}$ and $I_{D(B)}$ are equal to the A-side driver sink current and B-side driver sink current, respectively. It is important to note that in Equation 7 $V_{OL(A)} < V_{IL(B)}$ and in Equation 8 $V_{OL(B)}$ is $\geq V_{IL(A)}$ so $V_{OL(B)}$ is lowered to $V_{IL(A)}$ to satisfy the working operation of the I/O.

$$R_{pu} = \frac{V_{CC(A)} - V_{OL(A)} + V_{CC(B)} - V_{OL(A)}}{I_{D(A)}} = \frac{2.5\ V - 0.25\ V + 3.3\ V - 0.25\ V}{10\ mA} = 530\ \Omega \quad (7)$$

$$R_{pu} = \frac{V_{CC(A)} - V_{IL(A)} + V_{CC(B)} - V_{IL(A)}}{I_{D(B)}} = \frac{2.5\ V - 0.25\ V + 3.3\ V - 0.25\ V}{15\ mA} = 353\ \Omega \quad (8)$$

For this example the smallest resistance that can be used and still meet the V_{OL} and V_{IL} requirements is 530 Ω.

Table 3, Table 4 and Table 5 contain suggested minimum values of pull-up resistors for the PCA9306 and NVT20xx devices with typical voltage translation levels and drive currents. The calculated values assume that both drive currents are the same. $V_{OL} = V_{IL} = 0.1 \times V_{CC}$ and accounts for a ±5 % V_{CC} tolerance of the supplies, ±1 % resistor values. It should be noted that the resistor chosen in the final application should be equal to or larger than the values shown in Table 3, Table 4 and Table 5 to ensure that the pass voltage is less than 10 % of the V_{CC} voltage, and the external driver should be able to sink the total current from both pull-up resistors. When selecting the minimum resistor value in Table 3, Table 4 or Table 5, the drive current strength that should be chosen should be the lowest drive current seen in the application and account for any

1. The switch resistance is typically 3 Ω, but when calculating for R_{pu}, the switch resistance is negligible and can be assumed to be 0 Ω so that simplifications can be made.

drive strength current scaling with output voltage. For the GTL devices, the resistance table should be recalculated to account for the difference in ON resistance and bias voltage limitations between $V_{CC(B)}$ and $V_{CC(A)}$.

Table 3. Pull-up resistor minimum values, 3 mA driver sink current for PCA9306 and NVT20xx

A-side	B-side					
	1.2 V	**1.5 V**	**1.8 V**	**2.5 V**	**3.3 V**	**5.0 V**
1.0 V	$R_{pu(A)}$ = 750 Ω $R_{pu(B)}$ = 750 Ω	$R_{pu(A)}$ = 845 Ω $R_{pu(B)}$ = 845 Ω	$R_{pu(A)}$ = 976 Ω $R_{pu(B)}$ = 976 Ω	$R_{pu(A)}$ = none $R_{pu(B)}$ = 887 Ω	$R_{pu(A)}$ = none $R_{pu(B)}$ = 1.18 kΩ	$R_{pu(A)}$ = none $R_{pu(B)}$ = 1.82 kΩ
1.2 V		$R_{pu(A)}$ = 931 Ω $R_{pu(B)}$ = 931 Ω	$R_{pu(A)}$ = 1.02 kΩ $R_{pu(B)}$ = 1.02 kΩ	$R_{pu(A)}$ = none $R_{pu(B)}$ = 887 Ω	$R_{pu(A)}$ = none $R_{pu(B)}$ = 1.18 kΩ	$R_{pu(A)}$ = none $R_{pu(B)}$ = 1.82 kΩ
1.5 V			$R_{pu(A)}$ = 1.1 kΩ $R_{pu(B)}$ = 1.1 kΩ	$R_{pu(A)}$ = none $R_{pu(B)}$ = 866 Ω	$R_{pu(A)}$ = none $R_{pu(B)}$ = 1.18 kΩ	$R_{pu(A)}$ = none $R_{pu(B)}$ = 1.78 kΩ
1.8 V				$R_{pu(A)}$ = 1.47 kΩ $R_{pu(B)}$ = 1.47 kΩ	$R_{pu(A)}$ = none $R_{pu(B)}$ = 1.15 kΩ	$R_{pu(A)}$ = none $R_{pu(B)}$ = 1.78 kΩ
2.5 V					$R_{pu(A)}$ = 1.96 kΩ $R_{pu(B)}$ = 1.96 kΩ	$R_{pu(A)}$ = none $R_{pu(B)}$ = 1.78 kΩ
3.3 V						$R_{pu(A)}$ = none $R_{pu(B)}$ = 1.74 kΩ

Table 4. Pull-up resistor minimum values, 10 mA driver sink current for PCA9306 and NVT20xx

A-side	B-side					
	1.2 V	**1.5 V**	**1.8 V**	**2.5 V**	**3.3 V**	**5.0 V**
1.0 V	$R_{pu(A)}$ = 221 Ω $R_{pu(B)}$ = 221 Ω	$R_{pu(A)}$ = 255 Ω $R_{pu(B)}$ = 255 Ω	$R_{pu(A)}$ = 287 Ω $R_{pu(B)}$ = 287 Ω	$R_{pu(A)}$ = none $R_{pu(B)}$ = 267 Ω	$R_{pu(A)}$ = none $R_{pu(B)}$ = 357 Ω	$R_{pu(A)}$ = none $R_{pu(B)}$ = 549 Ω
1.2 V		$R_{pu(A)}$ = 274 Ω $R_{pu(B)}$ = 274 Ω	$R_{pu(A)}$ = 309 Ω $R_{pu(B)}$ = 309 Ω	$R_{pu(A)}$ = none $R_{pu(B)}$ = 267 Ω	$R_{pu(A)}$ = none $R_{pu(B)}$ = 357 Ω	$R_{pu(A)}$ = none $R_{pu(B)}$ = 549 Ω
1.5 V			$R_{pu(A)}$ = 332 Ω $R_{pu(B)}$ = 332 Ω	$R_{pu(A)}$ = none $R_{pu(B)}$ = 261 Ω	$R_{pu(A)}$ = none $R_{pu(B)}$ = 348 Ω	$R_{pu(A)}$ = none $R_{pu(B)}$ = 536 Ω
1.8 V				$R_{pu(A)}$ = 442 Ω $R_{pu(B)}$ = 442 Ω	$R_{pu(A)}$ = none $R_{pu(B)}$ = 348 Ω	$R_{pu(A)}$ = none $R_{pu(B)}$ = 536 Ω
2.5 V					$R_{pu(A)}$ = 590 Ω $R_{pu(B)}$ = 590 Ω	$R_{pu(A)}$ = none $R_{pu(B)}$ = 523 Ω
3.3 V						$R_{pu(A)}$ = none $R_{pu(B)}$ = 523 Ω

Table 5. Pull-up resistor minimum values, 15 mA driver sink current for PCA9306 and NVT20xx

A-side	B-side					
	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	5.0 V
1.0 V	$R_{pu(A)}$ = 147 Ω $R_{pu(B)}$ = 147 Ω	$R_{pu(A)}$ = 169 Ω $R_{pu(B)}$ = 169 Ω	$R_{pu(A)}$ = 191 Ω $R_{pu(B)}$ = 191 Ω	$R_{pu(A)}$ = none $R_{pu(B)}$ = 178 Ω	$R_{pu(A)}$ = none $R_{pu(B)}$ = 237 Ω	$R_{pu(A)}$ = none $R_{pu(B)}$ = 365 Ω
1.2 V		$R_{pu(A)}$ = 182 Ω $R_{pu(B)}$ = 182 Ω	$R_{pu(A)}$ = 205 Ω $R_{pu(B)}$ = 205 Ω	$R_{pu(A)}$ = none $R_{pu(B)}$ = 178 Ω	$R_{pu(A)}$ = none $R_{pu(B)}$ = 237 Ω	$R_{pu(A)}$ = none $R_{pu(B)}$ = 365 Ω
1.5 V			$R_{pu(A)}$ = 221 Ω $R_{pu(B)}$ = 221 Ω	$R_{pu(A)}$ = none $R_{pu(B)}$ = 174 Ω	$R_{pu(A)}$ = none $R_{pu(B)}$ = 232 Ω	$R_{pu(A)}$ = none $R_{pu(B)}$ = 357 Ω
1.8 V				$R_{pu(A)}$ = 294 Ω $R_{pu(B)}$ = 294 Ω	$R_{pu(A)}$ = none $R_{pu(B)}$ = 232 Ω	$R_{pu(A)}$ = none $R_{pu(B)}$ = 357 Ω
2.5 V					$R_{pu(A)}$ = 392 Ω $R_{pu(B)}$ = 392 Ω	$R_{pu(A)}$ = none $R_{pu(B)}$ = 357 Ω
3.3 V						$R_{pu(A)}$ = none $R_{pu(B)}$ = 348 Ω

7. How to design for maximum frequency operation

The maximum frequency is limited by the minimum pulse width LOW and HIGH as well as rise time and fall time. See Equation 9 as an example of the maximum frequency. The rise and fall times are shown in Figure 10.

$$f_{max} = \frac{1}{t_{LOW(min)} + t_{HIGH(min)} + t_{r(actual)} + t_{f(actual)}} \quad (9)$$

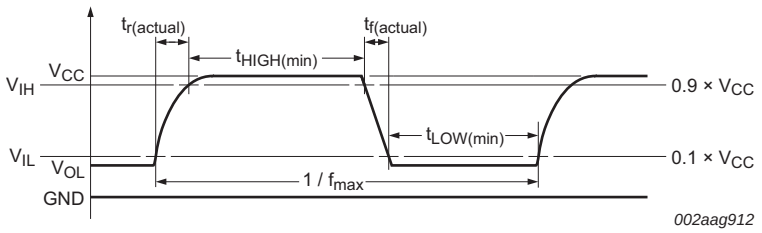


Fig 10. An example waveform for maximum frequency

The rise and fall times are dependent upon translation voltages, the drive strength, the total node capacitance ($C_{L(tot)}$) and the pull-up resistors (R_{PU}) that are present on the bus. The node capacitance is the addition of the PCB trace capacitance and the device capacitance that exists on the bus. Because of the dependency of the external components, PCB layout and the different device operating states the calculation of rise and fall times is complex and has several inflection points along the curve.

The main component of the rise and fall times is the RC time constant of the bus line when the device is in its two primary operating states: when device is in the ON state and it is low-impedance, the other is when the device is OFF isolating the A-side from the B-side.

A description of the fall time applied to either An or Bn output going from HIGH to LOW is as follows. Whichever side is asserted first, the B-side down must discharge to the $V_{CC(A)}$ voltage. The time is determined by the pull-up resistor, pull-down driver strength and the capacitance. As the level moves below the $V_{CC(A)}$ voltage, the channel resistance drops so that both A and B sides equal. The capacitance on both sides is connected to form the total capacitance and the pull-up resistors on both sides combine to the parallel equivalent resistance. The R_{on} of the device is small compared to the pull-up resistor values, so its effect on the pull-up resistance can be neglected and the fall is determined by the driver pulling the combined capacitance and pull-up resistor currents. An estimation of the actual fall time seen by the device is equal to the time it takes for the B-side to fall to the $V_{CC(A)}$ voltage and the time it takes for both sides to fall from the $V_{CC(A)}$ voltage to the V_{IL} level.

A description of the rise time applied to either An or Bn output going from LOW to HIGH is as follows. When the signal level is LOW, the R_{on} is at its minimum, so the A and B sides are essentially one node. They will rise together with an RC time constant that is the sum of all the capacitance from both sides and the parallel of the resistance from both sides. As the signal approaches the $V_{CC(A)}$ voltage, the channel resistance goes up and the waveforms separate, with the B side finishing its rise with the RC time constant of the B side. The rise to $V_{CC(A)}$ is essentially the same for both sides.

There are some basic guidelines to follow that will help maximize the performance of the device:

- Keep trace length to a minimum by placing the NVT device close to the processor.
- The signal round trip time on trace should be shorter than the rise or fall time of signal to reduce reflections.
- The faster the edge of the signal, the higher the chance for ringing.
- The higher drive strength controlled by the pull-up resistor (up to 15 mA), the higher the frequency the device can use.

The system designer must design the pull-up resistor value based on external current drive strength and limit the node capacitance (minimize the wire, stub, connector and trace length) to get the desired operation frequency result.

8. How to design for similar voltage levels from two different power domains

An example of a server application solving two different power supply sources is shown in Figure 11. Both power domains are nominally at the same potential, where the signal line crosses power supply domains that under normal operation would be at 3.3 V. However, one supply could be at 3.0 V (–10 %) and the other at 3.6 V (+10 %), or one could be experiencing a power failure while the other domain is trying to operate. NVT2003 is configured such that a second reference transistor, made from one of its channel transistors, with its A1 connected to V_{CC1} and B1 connected to a voltage supply V_{CC2} that is at least 1 V above the maximum possible for either $V_{CC(A)}$ or V_{CC1}. Then if either pull-up voltage is at 0 V, the channels are disabled and in high-impedance state, otherwise the EN (gate) is biased to a threshold above the lower supply voltage either $V_{CC(A)}$ or V_{CC1} and the pass voltage is therefore limited to the lower of either A side or B side voltage. Pull-up resistors are required on both sides.

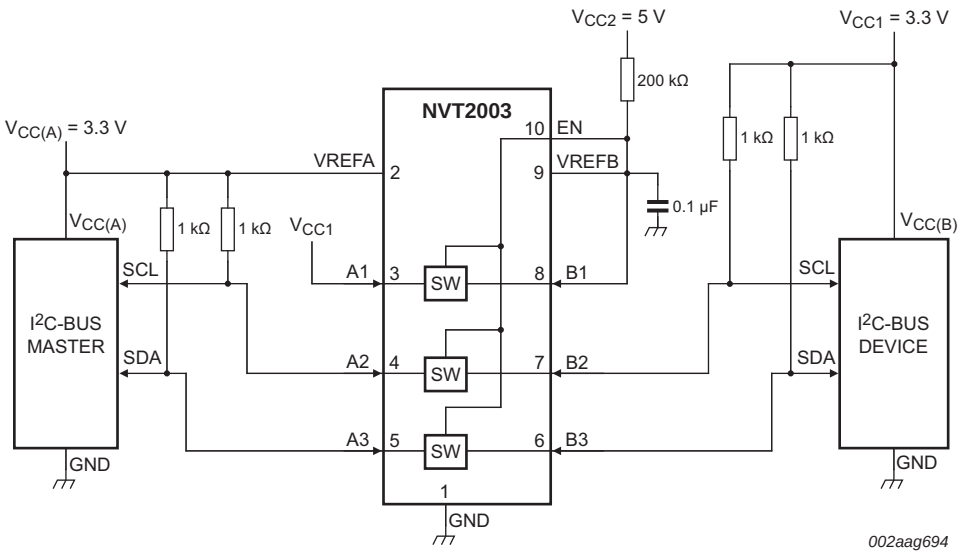


Fig 11. NVT2003 application for different 3.3 V power sources

9. NVT20xx demo boards

These demo boards are designed to let customers evaluate all of NVT20xx bidirectional voltage level translator.

- Simple to evaluate each NVT device without additional components
- All Bn I/O pins on high voltage right hand side always have 10 kΩ pull-up resistors to VREFB
- All An I/O pins on low voltage left hand side with jumper option have 10 kΩ pull-up resistors to VREFA
- Jumper J1 (3 pins) to control NVT device enable (pin 2-3 on) or disable (pin 1-2 on)
- Easy to apply high voltage VREFB/GND and Bn signals on right hand side header
- Easy to apply low voltage VREFA/GND and An signals on left hand side header

There are seven demo boards available for NVT20xx family an example of three boards is shown in Figure 12.

- The OM13315 demo board is designed for NVT2001GM.
- The OM13316 demo board is designed for NVT2004TL.
- The OM13317 demo board is designed for NVT2008PW.
- The OM13318 demo board is designed for NVT2002DP.
- The OM13319 demo board is designed for NVT2003DP.
- The OM13323 demo board is designed for NVT2006PW.
- The OM13324 demo board is designed for NVT2010PW.

For schematics and more information on the demo boards, please refer to the NVT user manual for each board.

019aac708

a. NVT2003DP (OM13319)

019aac709

b. NVT2004TL (OM13316)

019aac710

c. NVT2006PW (OM13323)

Fig 12. Bidirectional voltage level translators demo boards

10. Frequently asked questions

1. **Question:** The NVT schematic (Figure 2) makes these parts look like an array of NMOS transistors; are they?

   Answer: Yes, the NVT20xx are arrays of NMOS transistors with a common gate, they were designed as level shifters/clamps where the inherent matching is used by making one transistor a reference and the remaining transistors as level shifters/clamps. Not shown in the schematic are the ESD protection devices between each pin and ground.

2. **Question:** What is the difference between the NVT20xx and GTL2000/2002/2003/2010 devices?

   Answer: In the NVT schematic, VREFA on the NVT20xx is the same as SREF on the GTL20xx, EN on the NVT20xx is the same as GREF on the GTL20xx, VREFB on the NVT20xx is the same as DREF on the GTL20xx, I/O port An on the NVT20xx is the same as I/O port Sn on the GTL20xx, and I/O port Bn on the NVT20xx is the same as I/O port Dn on the GTL20xx. The NVT20xx is functionally equivalent to the GTL20xx, but the NVT20xx has lower channel ON-resistance (R_{on} = 3.5 Ω) over existing GTL devices (R_{on} = 6.5 Ω) and higher ESD protection exceeds 4 kV HBM.

3. **Question:** Can any one of the transistors in the array be used as the reference transistor?

   Answer: Yes, as shown in Figure 2, any transistor can be used as long as its Bn pin is connected to the EN pin and its associated An is used as the $V_{CC(A)}$. However, the VREFB pin is probably the easiest to use because of its close proximity to the EN pin.

4. **Question:** Are the An and Bn pins interchangeable?

   Answer: Yes, the An and Bn labels are merely for convenience in thinking about the device's I/O ports. The An pin could be used as a drain and the corresponding Bn pin used as a source. The 'n' indicates an I/O port number, which identifies a transistor number. Thus, A1 and B1 correspond to transistor 1.

5. **Question:** Are both the An and Bn ports 5 V I/O tolerant?

   Answer: Yes, both the ports are 5.5 V tolerant, and the EN pin is also 5.5 V tolerant.

6. **Question:** Do the NVT20xx devices isolate the capacitance in the line?

   Answer: No, the devices do not have this capability since the device is basically an array of NMOS transistors.

7. **Question:** What will be the typical propagation delay for NVT20xx device family?

   Answer: The NVT20xx family of devices have the propagation delay associated with a 5 Ω transistor ON-state for much of the swing. Thus, with a 50 pF load and a low resistance driver driving the transition and measuring both sides at the same voltage level (that is, 1.5 V), the delay is about 0.25 ns (5 Ω × 50 pF). If the delay wanted is from the low voltage side (1 V) where the measurement point is 1 V to CMOS at 5 V in the high voltage side, with a 2.5 V measurement voltage, then the delay is not the 0.25 ns of the NVT20xx family part. It is rather primarily the delay of the system, that is the RC time constant of the external pull-up resistor and the line capacitance, which determine the rise time between 1 V and 2.5 V. The fall time is not affected as much because the driver's effective resistance is very low compared to the external pull-up resistor, so the 2.5 V to 1 V transition is much faster than the rising transition.

8. **Question:** I am using a 3.3 V FPGA with an NVT device on some pins. The NVT device does the level conversion, either down to 1.8 V or up to 5 V. The pins from the NVT device go to a connector. There is a possibility that a human being touches it and there an ESD can occur. Will NVT prevent the FPGA from ESD? I think that the NVT device is ESD protected, am I right?

   Answer: The NVT20xx devices all have ESD protection > 4 kV HBM and they should absorb most of the energy from an ESD event. The NVT part on the connector will absorb the primary ESD energy, but we cannot guarantee that this will always protect the FPGA. Very little of the ESD energy may reach the FPGA, however.

9. **Question:** Due to the requirement of the voltage for the 200 kΩ pull-up at both the EN and VREFB pins that has to be at least 1.0 V higher than the $V_{CC(A)}$ voltage (1.8 V in this case), the voltage at the 200 kΩ pull-up resistor needs to be at least 2.8 V. The design does not have such voltage provided other than 1.8 V and 2.5 V. Can the NVT device be used?

   Answer: The device will work with 0.8 V differential, but the actual voltage seen on the lower side may not be what $V_{CC(A)}$ sets. Example would be one side at 3.3 V and the other at 1.8 V; you will always see 3.3 V and 1.8 V. If one side is at 3.3 V and the other at 2.5 V, then you will always see 3.3 V, but may see less than 2.5 V on the other side. The problem is not that the 2.5 V side would be above 2.5 V, but rather that it might only get as high as 2.3 V and that the exact value will vary from part to part and would be between 2.3 V and 2.5 V.

   In this specific case, the 1.8 V low-voltage side may only reach to 1.5 V when biased with the 2.5 V supply. An external pull-up resistor to 1.8 V supply could be used to make certain that it gets to 1.8 V.

10. **Question:** We use only three bits on the NVT2004. One of the bits is ‘not connected’ (A4) and B4 is open. Is this OK or should they be tied to EN?

    Answer: There are several acceptable ways of dealing with unused data paths and treating them as ‘not connected’ is probably the easiest. It is recommended that pads be included on the circuit board for the unused pins so that after soldering the part will be firmly attached. Alternatively, the unused Bn and An pins can be connected together and tied to GND. It is not recommended connecting unused paths to EN.

11. **Question:** I use three NVT2010 devices for translating 30 signals from 3.3 V to 1.8 V. Can the 200 kΩ resistor be shared by all three NVT2010 EN and VREFB pins, or do I need three 200 kΩ resistors? What is the recommended value for the capacitor next to the 200 kΩ resistor?

    Answer: It would be best to use three different resistors, because different packages may not have identical characteristics and separate resistors/biasing allow the circuit to compensate for these differences. Sharing one resistor would not work well. A 0.1 μF capacitor is recommended. Note that the capacitor stabilizes the gate node but also slows its power-up: with a 200 kΩ resistor, it will take on the order of 100 ms to get to the correct clamp level with a 0.1 μF capacitor. Since the gate node has over 100 pF capacitance, the capacitor needs to be in at least the nF range to do anything. If you do not have any speed constraint at power-up, then 0.1 μF would be safe enough.

12. **Question:** Can I use the NVT2006 to level shift from 1.8 V to 3.3 V and from 1.8 V to 5 V at the same time?

    Answer: Yes, as long as the LOW side high voltage is the same for both translations as 1.8 V. In this case, the VREFA can be connected to 1.8 V and different transistors used, that is, source side on the 1.8 V level and the drain of one at 3.3 V and the drain of the other at 5.0 V as shown in Figure 4. The pull-up resistors would need to be sized so as not to exceed the maximum allowed current (that is, 15 mA) for the NVT device.

13. **Question:** We need a translator to convert signals from 5 V to 3.3 V and vice-versa. But the drivers are not open-drain. In this case, can I use NVT2010?

    Answer: If the drivers are not open-drain, your system needs to integrate some flag between the driving devices so there is no conflict by having one device driving a HIGH level while at the same time the other one is driving a LOW level. There needs to be a way to prevent bus contention, otherwise the devices would be damaged. With that in mind, the NVT2010 can be used.

14. **Question:** Why was the low voltage limit of the NVT20xx devices set at 1 V? Could it be used at 0.8 V?

    Answer: The low voltage limit is not in the DC specifications but the bullet under 'Features' states level translation down to 1 V. The NVT20xx devices' $V_{CC(A)}$ is not recommended below 1 V to insure a low ON resistance. The problem with a $V_{CC(A)}$ voltage lower than 1 V is that the gate overdrive. This means that the NMOS transistor does not turn on as hard and so the ON resistance increases. Once you get below a certain gate overdrive, the ON resistance increases rapidly. The part will still be functional, but the ON resistance will be higher.

15. **Question:** We want to use the NVT2010 to translate signals from 1.5 V to 3.3 V, so our settings will be $V_{CC(A)}$ = 1.5 V, $V_{CC(B)}$ = 3.3 V. But we use only 6 bits of the 10-bit NVT2010, so there are 4 bits unused. We plan to use these other 4 bits for signal translation from 3.3 V to 5 V. Looking through the application note we know that if the $V_{CC(B)}$ is 3.3 V, then the NVT2010 can support both 3.3 V and 5 V output mix on the B side. But is it suitable for $V_{CC(A)}$ to be changed to 3.3 V so that the input will support both a 1.5 V and 3.3 V input mix on the A side?

    Answer: As shown in Figure 13, to protect the 1.5 V parts the $V_{CC(A)}$ must stay at 1.5 V and you will have to rely on the 3.3 V pull-up on the A side and the 5 V pull-up on the B side to get the HIGH levels since the path will be essentially cut off above 1.5 V. It is possible to mix the voltages as proposed but the $V_{CC(A)}$ must be 1.5 V and the resistors on both the 3.3 V and 5 V sides determine the HIGHs with the LOW being passed through the NVT2010 (1.5 V pull-up resistor on A side is optional).

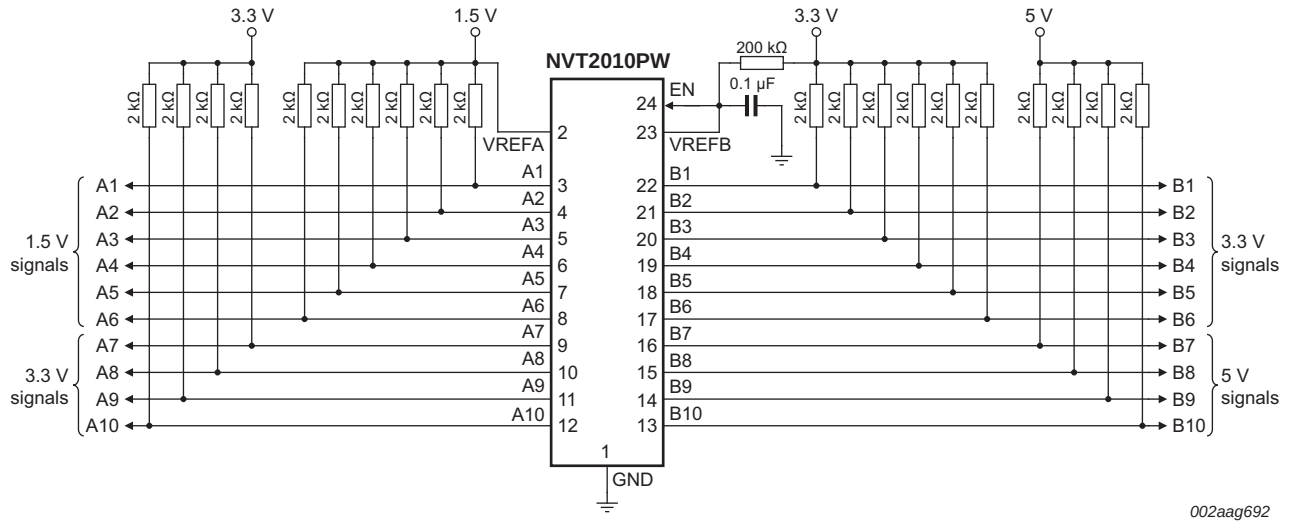


Fig 13. Application diagram for multiple voltages

16. **Question:** Is it possible to have the NVT2010 with 2.5 V and 3.3 V on one side and 5 V on the other side?

    Answer: Yes, if the 2.5 V and 3.3 V low side voltages are present at different times/applications, the VREFA could be used to connect to the current low side voltage. If both 2.5 V and 3.3 V voltages are present at the same time on the low voltage side with 5.0 V on the high voltage side, the VREFA will need to be connected to the lowest voltage, 2.5 V in this case, and the voltage that will be passed on the 3.3 V pins would be 2.5 V. Pull-up resistors could be used on the 3.3 V pins to achieve 3.3 V. The uni-directional or bidirectional voltage can be applied on a per channel basis. The idea of bidirectional is that there are drivers on both sides of the NVT2010 that can be active, so the signal can flow in either direction. If the outputs are totem pole outputs, some mechanism is required to prevent the contention of a HIGH level on one side with a LOW level on the other. The use of open-drain outputs eliminates the possibility of such a contention. Uni-directional means only one side of each channel has a driver so contention is not possible. Different channels in the same NVT2010 can be operated as bidirectional, uni-directional up translation or uni-directional down translation, and the HIGH side voltages can differ, but the VREFA must be connected to the LOW side voltage in order to clamp to that voltage.

17. **Question:** I have been looking at using the NVT2010 for a 2.5 V FPGA to 5 V sensor drive. Here's my configuration: the FPGA has to drive seven control signals to a 5 V part. The 5 V part has three outputs that connect to the FPGA. The FPGA is not 5 V tolerant and cannot be configured to have open-drain outputs. What configuration would be best for me to use?

    Answer: The clamp voltage would be set at 2.5 V for $V_{CC(A)}$ and VREFB/EN are connected to 5 V with 200 kΩ pull-up resistor, then each An/Bn pair can be used in a uni-directional (either direction) or bidirectional mode where you just need to treat each An/Bn pair individually. So the seven 2.5 V to 5 V signals would have no pull-up resistors on the 2.5 V side that are driven with the totem pole outputs and you would need to put pull-up resistors on the 5 V side so the sensor input would see 5 V HIGH

when the FPGA is driving HIGH, or LOW when the FPGA is driving LOW. The three 5 V to 2.5 V signals would not need the pull-up resistor on the 5 V side if the sensor has totem pole outputs and you do not need pull-up resistors on the 2.5 V side.

18. **Question:** We are using the NVT2008 for the one-way level shifting from 3.3 V to 1.8 V. What is set-up time and the hold time of NVT2008?

    Answer: 'Set-up time' and 'hold time' refer to flip-flop or latch parts, so they have no meaning with respect to the NVT20xx parts.

19. **Question:** All transistor switches are OFF when both the EN and VREFB are LOW. It is specified that the input and the output are disconnected. When NVT20xx becomes this state, is this correct that all inputs and outputs of the NVT20xx become the high-impedance? Please let us know the maximum voltage we can induce to the I/O of NVT20xx when it is high-impedance. Can we induce the 5.5 V maximum to the I/O?

    Answer: If the EN/VREFB pins are at ground, the transistors in the NVT20xx are OFF and the path between each Bn and An is high-impedance, the maximum voltage can be induced up to 6 V.

20. **Question:** We have designed-in the NVT2002DP and would like to get the maximum power dissipation and the conditions under which we make that claim.

    Answer: About the maximum power dissipation, the NVT device is a passive device and there is no active control logic. This means there is no supply power (V_{DD}) required for device operation and only standby current or reference current (I_{ref}) for reference transistor and this current on VREFA is equal to the current on VREFB (but opposite in sign), which is equal to the current through the external 200 kΩ resistor. For example, the worst-case is if VREFA = 1.0 V, $V_{CC(B)}$ = 5 V, R = 200 kΩ, and assuming VREFB ~1.8 V, then
    ($V_{CC(B)}$ − VREFB) / 200 kΩ = (5 V − 1.8 V) / 200 kΩ = 16 μA. But each pass transistor's channel is limited to 15 mA (maximum) with ON-state resistor about 5 Ω (maximum), so the maximum power dissipation is
    $P = I^2R = 225 \times 10^{-6} \times 5\ \Omega = 1.125$ mW per channel (maximum).

21. **Question:** Fall time (signal from HIGH to LOW) is dominated by the external pull-down driver with only a slight pass transistor R_{on} (5 Ω) addition. Is this right?

    Answer: When the signal is HIGH the channel is essentially OFF, so whichever side falls first the transition down to the $V_{CC(A)}$ voltage will be determined by the pull-down driver and the local capacitance. As the level moves below the $V_{CC(A)}$ voltage, the channel resistance drops and the capacitance on both sides are connected to form the total capacitance and the pull-up resistors on both sides combine to the parallel equivalent resistance. The R_{on} is small compared to the pull-up resistor values, so its effect on the pull-up resistance can be ignored and the fall is determined by the driver pulling the combined capacitance and pull-up currents LOW. This falling edge is essentially the same on both sides delayed by a few hundred ps.

22. **Question:** Rise time is dominated by the $R_{PU} \times C_L$. Is this rise time applied to either An or Bn output from LOW-to-HIGH?

    Answer: When the signal level is LOW, the R_{on} will be at its minimum. The A and B sides are essentially one node, so to within a few hundred ps they rise together with an RC that is the sum of all the capacitance from both sides and the parallel of the R_{PU} from both sides. As the signal gets close to the $V_{CC(A)}$ voltage the channel resistance goes up and the waveforms separate, with the A side finishing its rise with the RC of the A side and the B side finishing its rise with the RC of the B side.

23. **Question:** How to calculate the rise time if there is no pull-up resistor?

    Answer: It is assumed that you mean no pull-up on the low voltage side (An), as described above the rise to nearly $V_{CC(A)}$ is essentially the same for both sides. Since the measurement point for propagation is almost always 50 % of the swing, the fact that the final rise slows down exponentially is not relevant.

11. Abbreviations

Table 6. Abbreviations

Acronym	Description
ASIC	Application-Specific Integrated Circuit
CMOS	Complementary Metal-Oxide Semiconductor
CPU	Central Processing Unit
ESD	ElectroStatic Discharge
FET	Field-Effect Transistor
FPGA	Field Programmable Gate Array
GTL	Gunning Transceiver Logic
HBM	Human Body Model
I^2C-bus	Inter-Integrated Circuit-bus
I/O	Input/Output
NMOS	Negative-channel Metal-Oxide Semiconductor
NVT	NXP Voltage Translator
PCB	Printed-Circuit Board
RC	Resistor-Capacitor network
SMBus	System Management Bus
SPI	Serial Peripheral Interface

12. References

[1] **UM10539, “NVT2003DP, NVT2004TL and NVT2006PW demo boards” —** user manual; NXP Semiconductors; www.nxp.com/documents/user_manual/UM10539.pdf

[2] **UM10540, “NVT2001GM and NVT2002DP demo boards” —** user manual; NXP Semiconductors; www.nxp.com/documents/user_manual/UM10540.pdf

[3] **UM10541, “NVT2008PW and NVT2010PW demo boards” —** user manual; NXP Semiconductors; www.nxp.com/documents/user_manual/UM10541.pdf

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